What is claimed is:

1. A method of writing data to a row of single transistor memory cells wherein an applied gate voltage when writing a "0" is different than an applied gate voltage when writing a "1."

2. The method of claim 1 wherein writing data comprises writing data to single transistor floating-body memory cells.

3. The method of claim 1 further comprising applying drain voltages to either charge or discharge bodies of the single transistor memory cells.

4. The method of claim 3 wherein applying a drain voltage to charge bodies comprises creating impact ionization currents.

5. The method of claim 3 wherein applying a drain voltage to discharge bodies comprises creating a voltage differential to turn on a diode.

6. The method of claim 1 wherein the applied gate voltage when writing a "0" is less than the applied gate voltage when writing a "1."

7. A method comprising writing data to floating-body memory cells in two phases, wherein each of the two phases utilizes a different word line voltage on a word line.

8. The method of claim 7 wherein a first phase writes to a first subset of memory cells coupled to the word line.

9. The method of claim 8 wherein the first phase discharges floating bodies of the first subset of memory cells.

10. The method of claim 8 wherein the first phase comprises reducing a voltage on at least one bit line to turn on a diode formed at least partially by a floating body of a transistor.

11. The method of claim 8 wherein a second phase writes to a second subset of memory cells coupled to the word line.

12. The method of claim 11 wherein the second phase charges floating bodies of the second subset of memory cells.

13. The method of claim 11 wherein:

the first phase includes providing a first drain voltage on the first subset of memory cells and a second drain voltage on cells other than the first subset; and

the second phase includes providing a third drain voltage on the second subset of memory cells and a fourth drain voltage on cells other than the second subset.

14. A method comprising:

providing a first voltage on a word line coupled to a plurality of memory cells;

writing "0" to at least one of the plurality of memory cells;

providing a second voltage on the word line; and

writing "1" to at least one of the plurality of memory cells.

15. The method of claim 14 wherein each of the plurality of memory cells includes a single transistor.

16. The method of claim 15 wherein the word line is coupled to gates of the single transistors.

17. The method of claim 15 wherein the second voltage is higher than the first voltage.

18. The method of claim 14 wherein each of the plurality of memory cells comprises a floating-body transistor.

19. The method of claim 14 wherein writing a "0" comprises providing a voltage on a bit line to turn on a diode.

20. The method of claim 14 wherein writing a "1" comprises providing a voltage on a bit line to generate an impact ionization current.

21. An apparatus comprising:

a row of memory cells; and

a word line driver coupled to the row of memory cells, the word line driver to generate a first voltage when writing a "0" and a second voltage when writing a "1."

22. The apparatus of claim 21 wherein the word line driver is adapted to generate at least three different voltages.

23. The apparatus of claim 22 wherein the word line driver is adapted to generate at least four different voltages.

24. The apparatus of claim 21 wherein the row of memory cells comprise floating-body transistors.

25. A memory device comprising:

floating-body single transistor memory cells;

a plurality of word line drivers coupled to the floating-body single transistor memory cells; and

a plurality of bit line drivers coupled to the floating-body single transistor memory cells;

wherein the memory device is adapted to perform two-phase writes in which the plurality of word line drivers drive a first voltage during a first phase to write one logical value, and the plurality of word line drivers drive a second voltage during a second phase to write a complementary logical value.

26. The memory device of claim 25 wherein the word line drivers are adapted to drive the first voltage during the first phase when coupled to a selected row, and to drive a third voltage during the first phase when coupled to an unselected row.

27. The memory device of claim 26 wherein the word line drivers are adapted to drive the second voltage during the second phase when coupled to a selected row, and to drive a fourth voltage during the second phase when coupled to an unselected row.

28. An electronic system comprising:

an antenna;

a first integrated circuit coupled to the antenna; and

a second integrated circuit including a memory device, the memory device comprising floating-body single transistor memory cells; a plurality of word line drivers coupled to the floating-body single transistor memory cells; and a plurality of bit line drivers coupled to the floating-body single transistor memory cells; wherein the memory device is adapted to perform two-phase writes in which the plurality of word line drivers drive a first voltage during a first phase to write one logical value, and the plurality of word line drivers drive a second voltage during a second phase to write a complementary logical value.

29. The electronic system of claim 28 wherein the word line drivers are adapted to drive the first voltage during the first phase when coupled to a selected row, and to drive a third voltage during the first phase when coupled to an unselected row.

30. The electronic system of claim 29 wherein the word line drivers are adapted to drive the second voltage during the second phase when coupled to a selected row, and to drive a fourth voltage during the second phase when coupled to an unselected row.